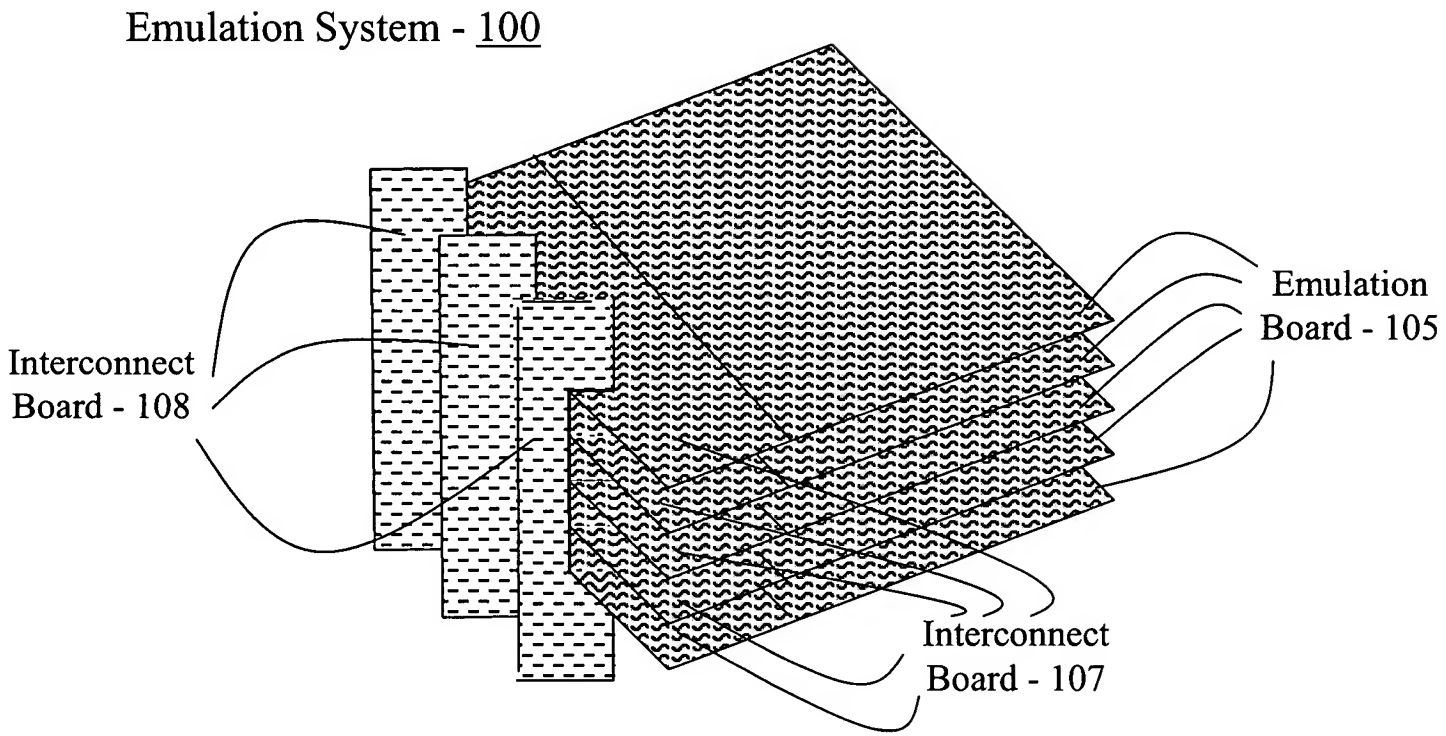
FIGURE 1


Emulation System - 100
Interconnect Board - 108
Emulation Board - 105
Interconnect Board - 107

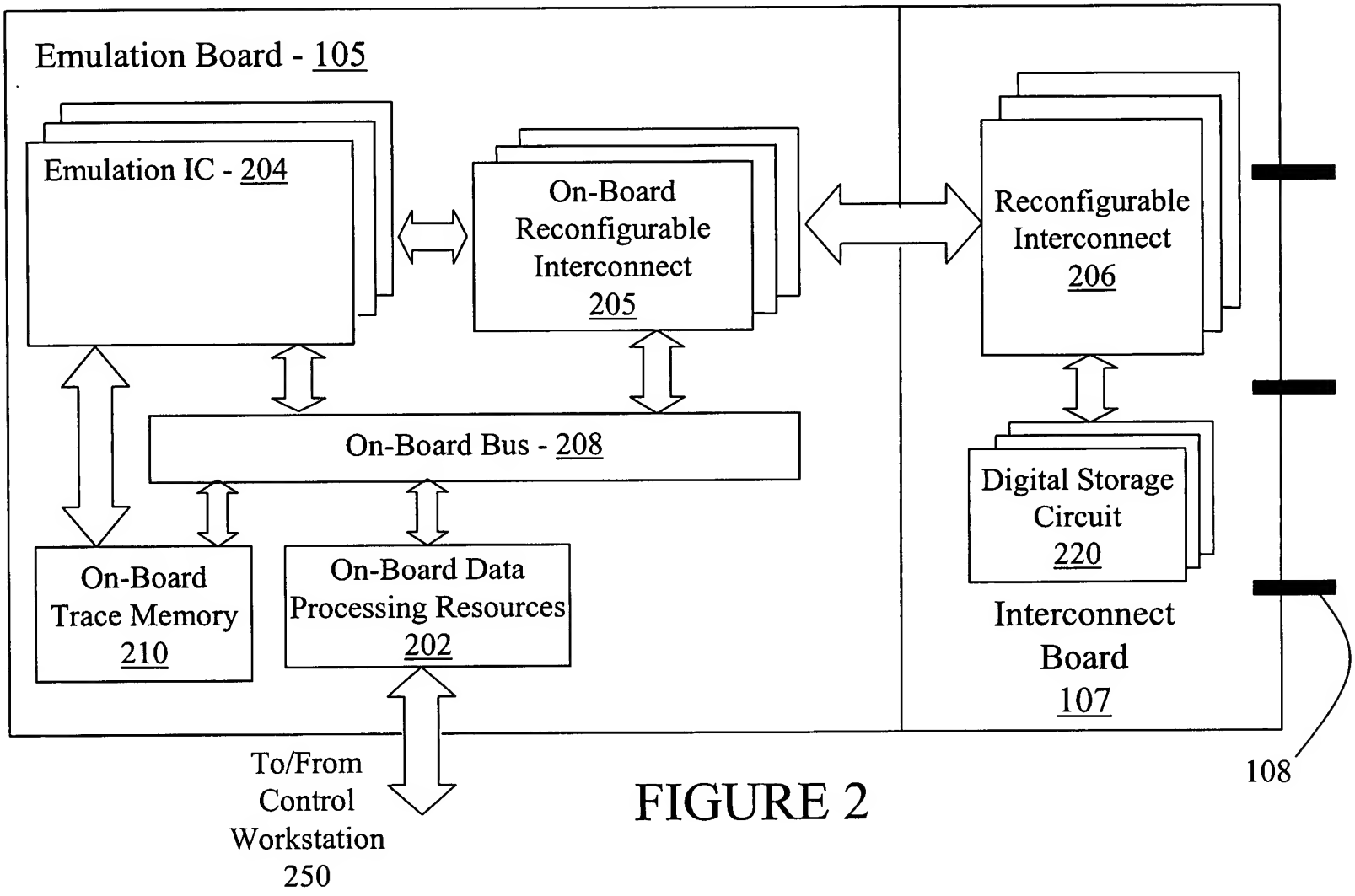

Emulation Board - 105
Emulation IC - 204
On-Board Reconfigurable Interconnect 205
Reconfigurable Interconnect 206
On-Board Bus - 208
Digital Storage Circuit 220
On-Board Trace Memory 210
On-Board Data Processing Resources 202
Interconnect Board 107
108
To/From Control Workstation 250

FIGURE 2

Figure 3

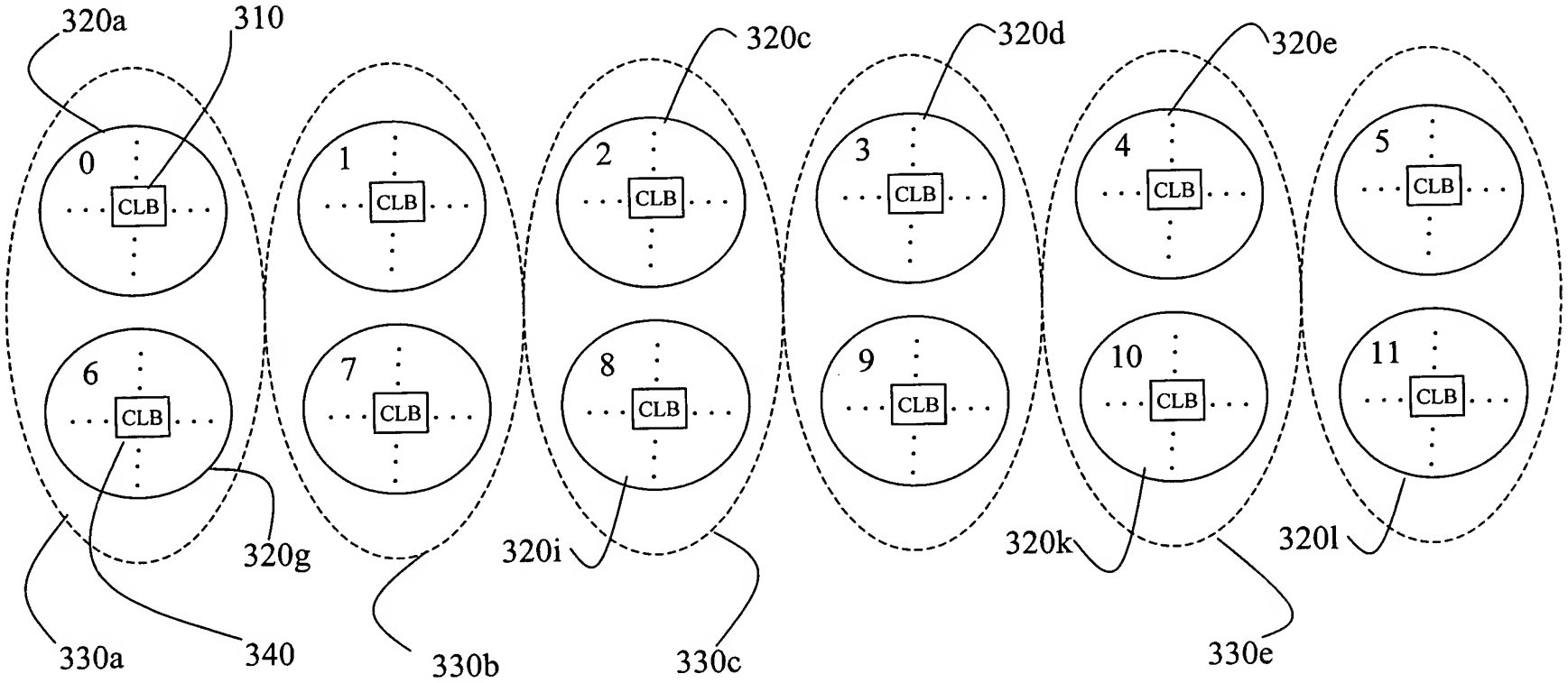
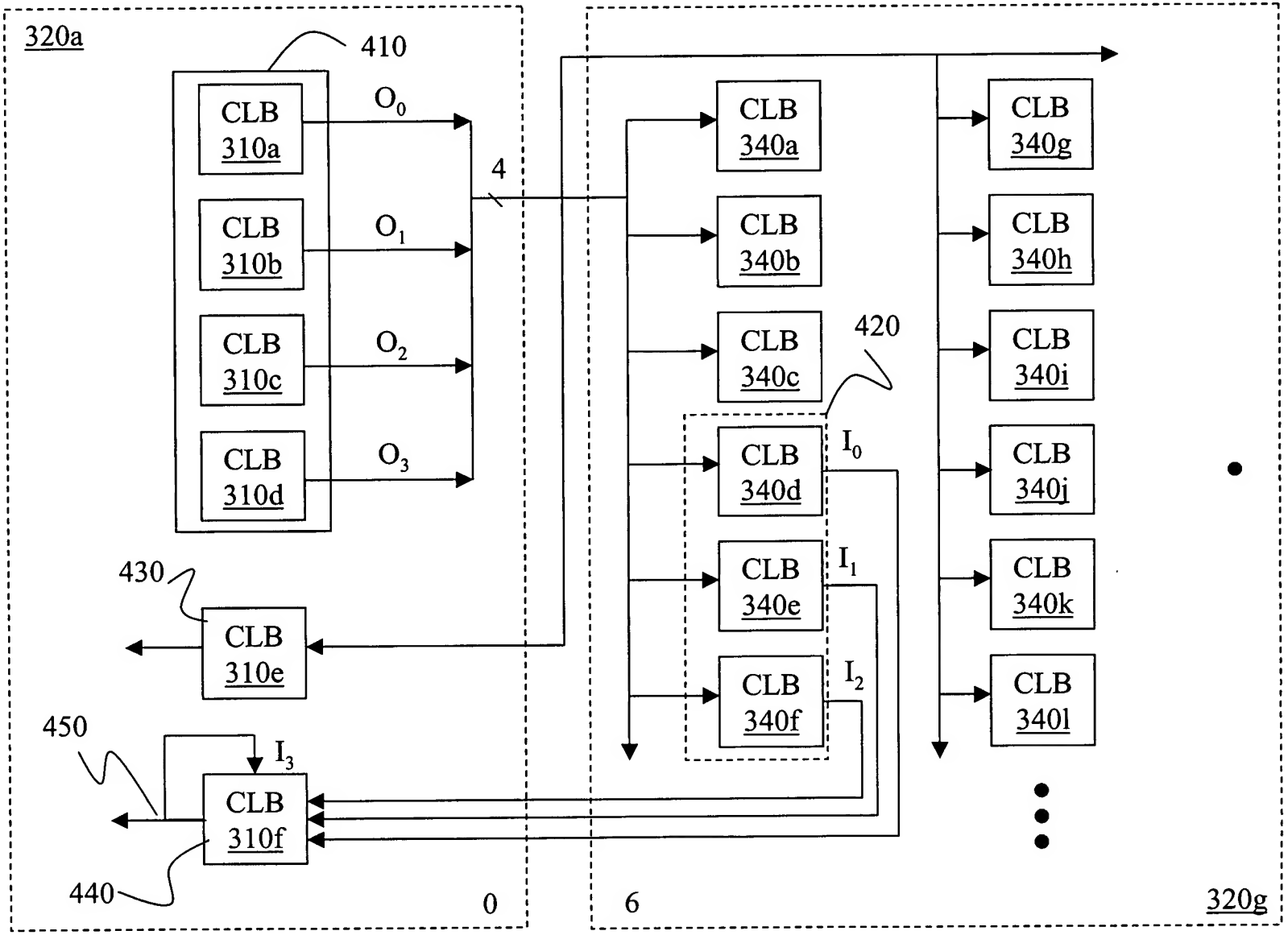

320a
310
320c
320d
320e
0
1
2
3
4
5
6
7
8
9
10
11
CLB
320g
320i
320k
320l
330a
340
330b
330c
330e

Figure 4


320a
410
CLB 310a
CLB 310b
CLB 310c
CLB 310d
O_0
O_1
O_2
O_3
4
430
CLB 310e
450
I_3
CLB 310f
440
0
6
CLB 340a
CLB 340b
CLB 340c
420
CLB 340d
CLB 340e
CLB 340f
I_0
I_1
I_2
CLB 340g
CLB 340h
CLB 340i
CLB 340j
CLB 340k
CLB 340l
320g

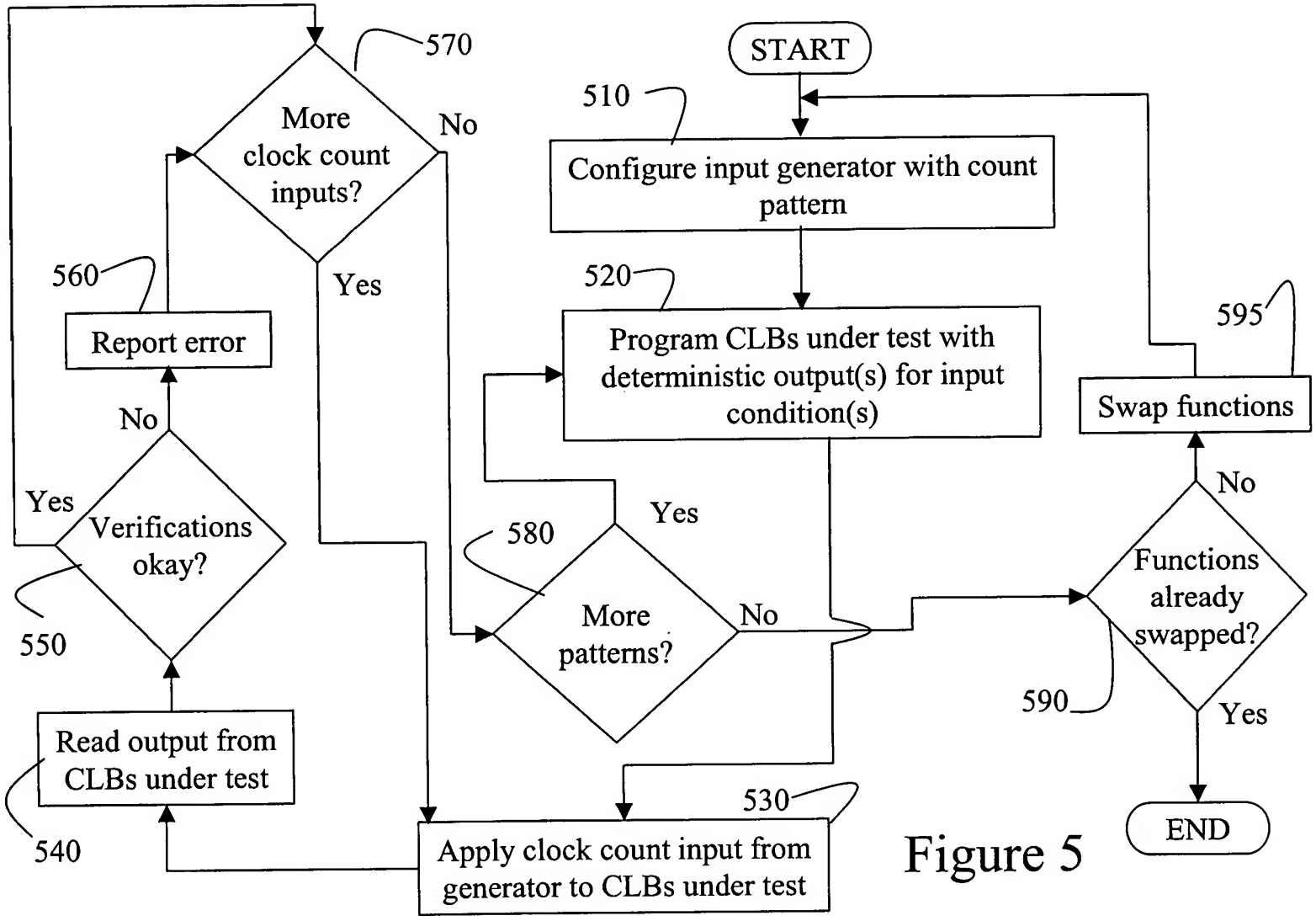

START
510
Configure input generator with count pattern
520
Program CLBs under test with deterministic output(s) for input condition(s)
530
Apply clock count input from generator to CLBs under test
540
Read output from CLBs under test
550
Verifications okay?
No
Yes
560
Report error
570
More clock count inputs?
No
Yes
580
More patterns?
Yes
No
590
Functions already swapped?
No
Yes
595
Swap functions
END

Figure 5

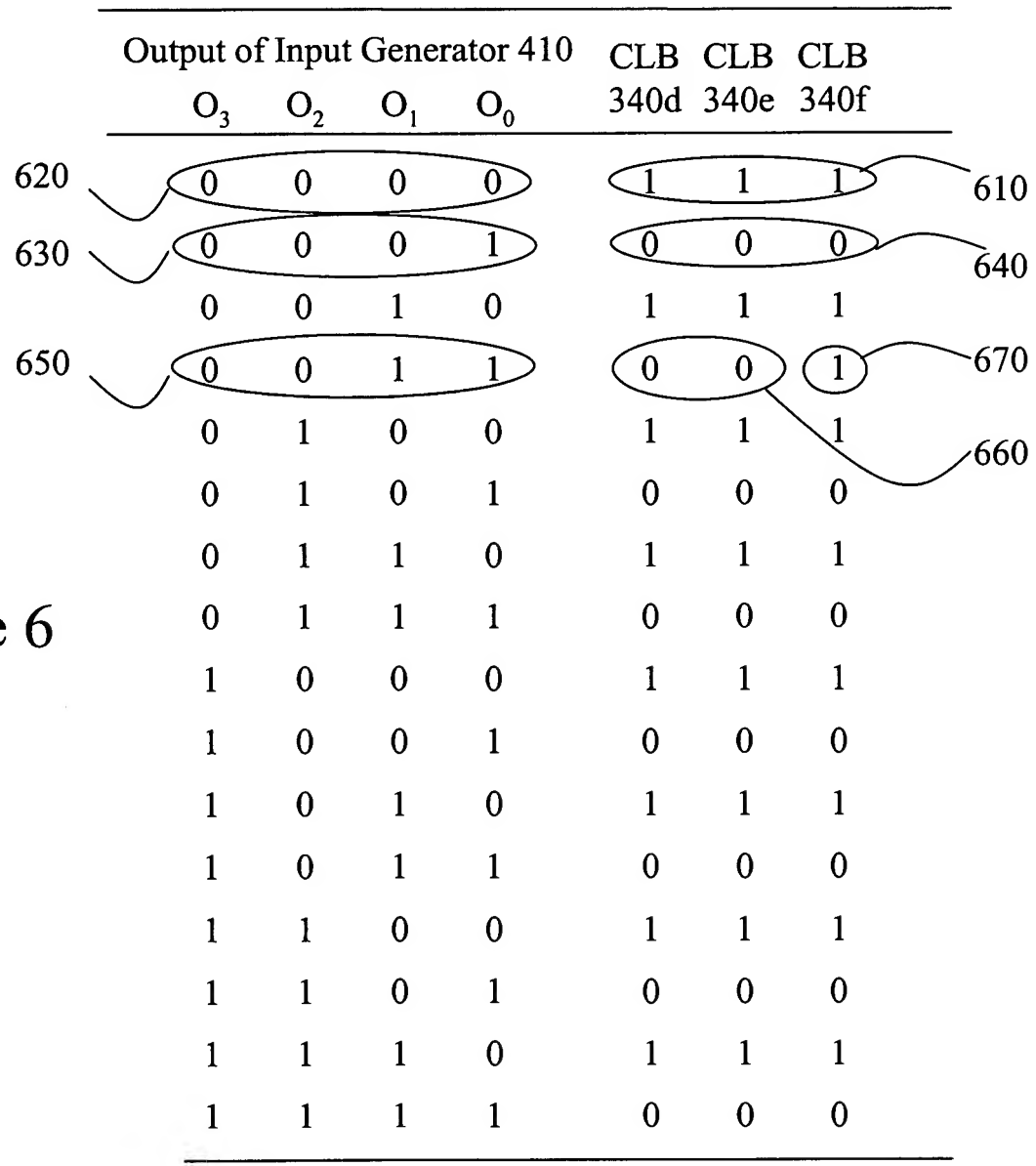

Output of Input Generator 410
O_3 O_2 O_1 O_0
CLB 340d CLB 340e CLB 340f
620
630
650
610
640
670
660
0 0 0 0 1 1 1
0 0 0 1 0 0 0
0 0 1 0 1 1 1
0 0 1 1 0 0 1
0 1 0 0 1 1 1
0 1 0 1 0 0 0
0 1 1 0 1 1 1
0 1 1 1 0 0 0
1 0 0 0 1 1 1
1 0 0 1 0 0 0
1 0 1 0 1 1 1
1 0 1 1 0 0 0
1 1 0 0 1 1 1
1 1 0 1 0 0 0
1 1 1 0 1 1 1
1 1 1 1 0 0 0

Figure 6

Figure 7

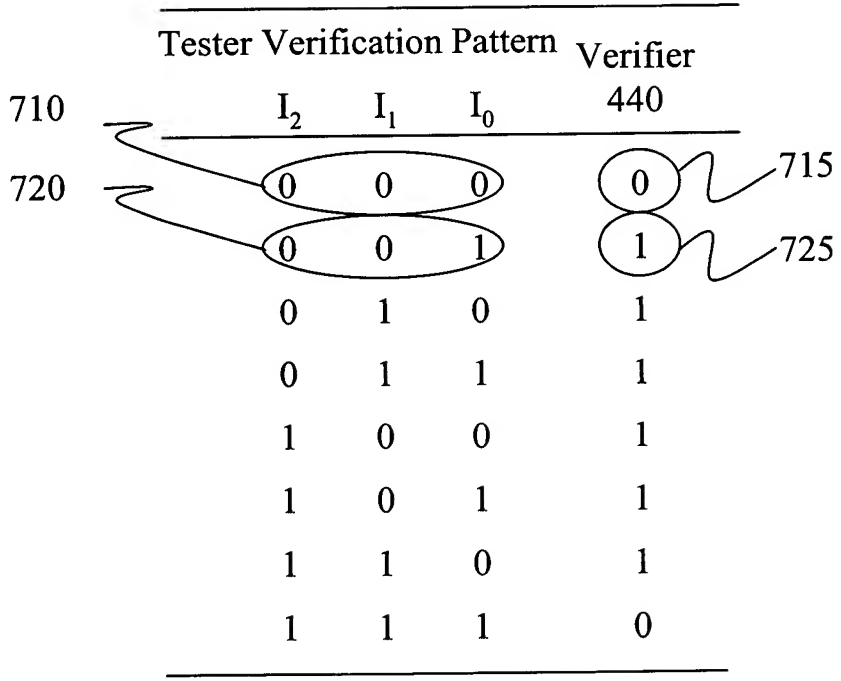
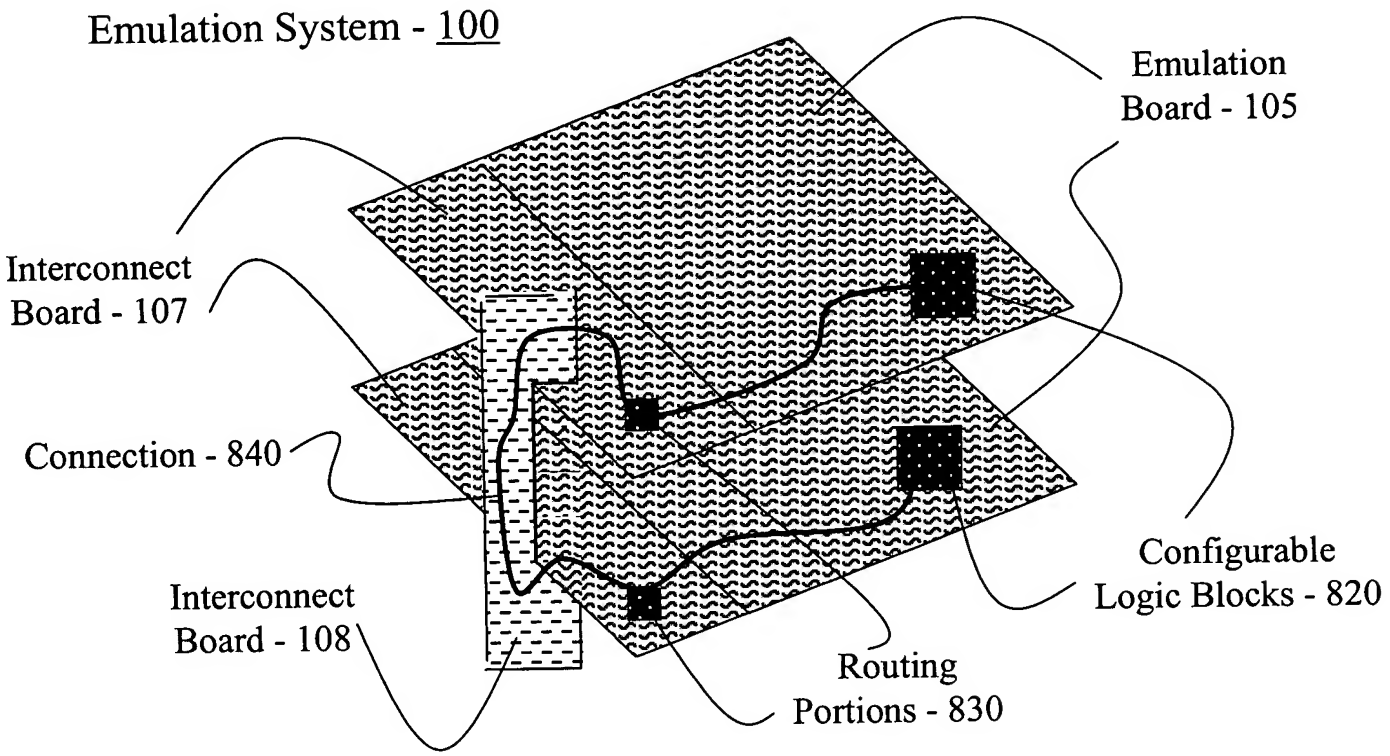

Tester Verification Pattern
Verifier
710
I_2 I_1 I_0
440
720
0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
1 0 1
1 1 0
1 1 1
0
1
1
1
1
1
1
0
715
725

FIGURE 8A


Emulation System - 100
Emulation Board - 105
Interconnect Board - 107
Connection - 840
Interconnect Board - 108
Routing Portions - 830
Configurable Logic Blocks - 820

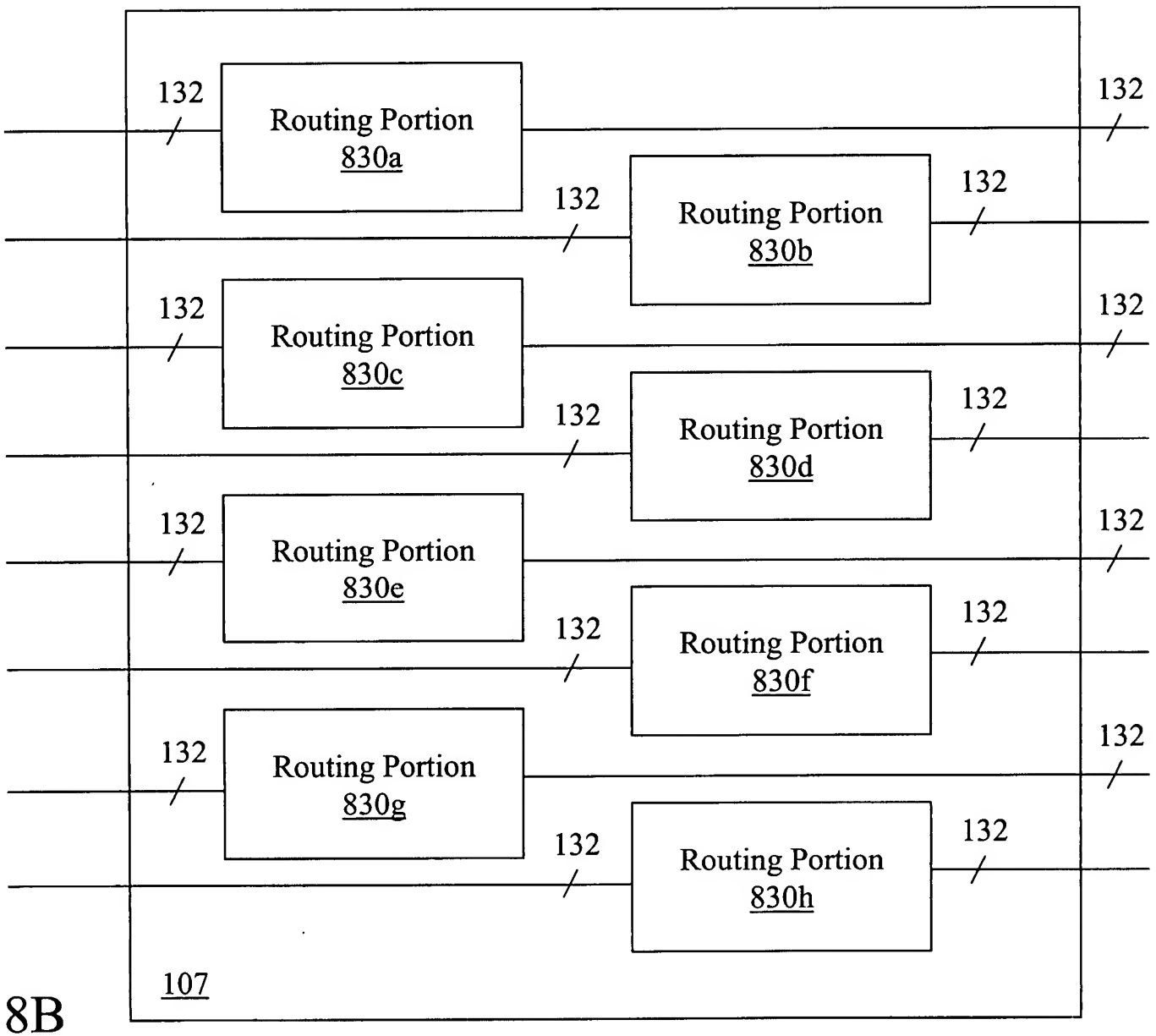

132
Routing Portion
830a
132
132
Routing Portion
830b
132
132
Routing Portion
830c
132
132
Routing Portion
830d
132
132
Routing Portion
830e
132
132
Routing Portion
830f
132
132
Routing Portion
830g
132
132
Routing Portion
830h
132
107

Figure 8B

Figure 9

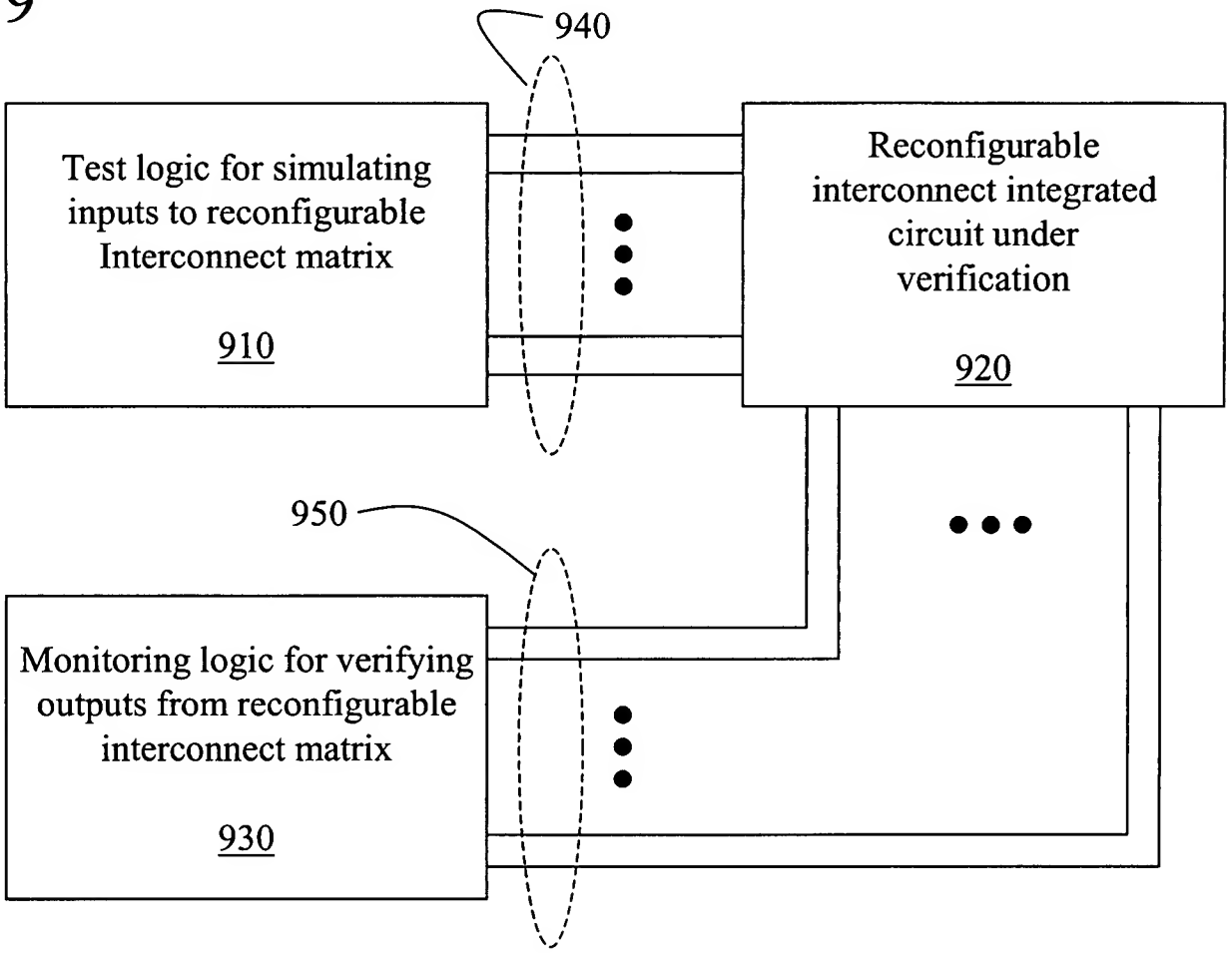

940
Test logic for simulating inputs to reconfigurable Interconnect matrix
910
Reconfigurable interconnect integrated circuit under verification
920
950
Monitoring logic for verifying outputs from reconfigurable interconnect matrix
930

Figure 10

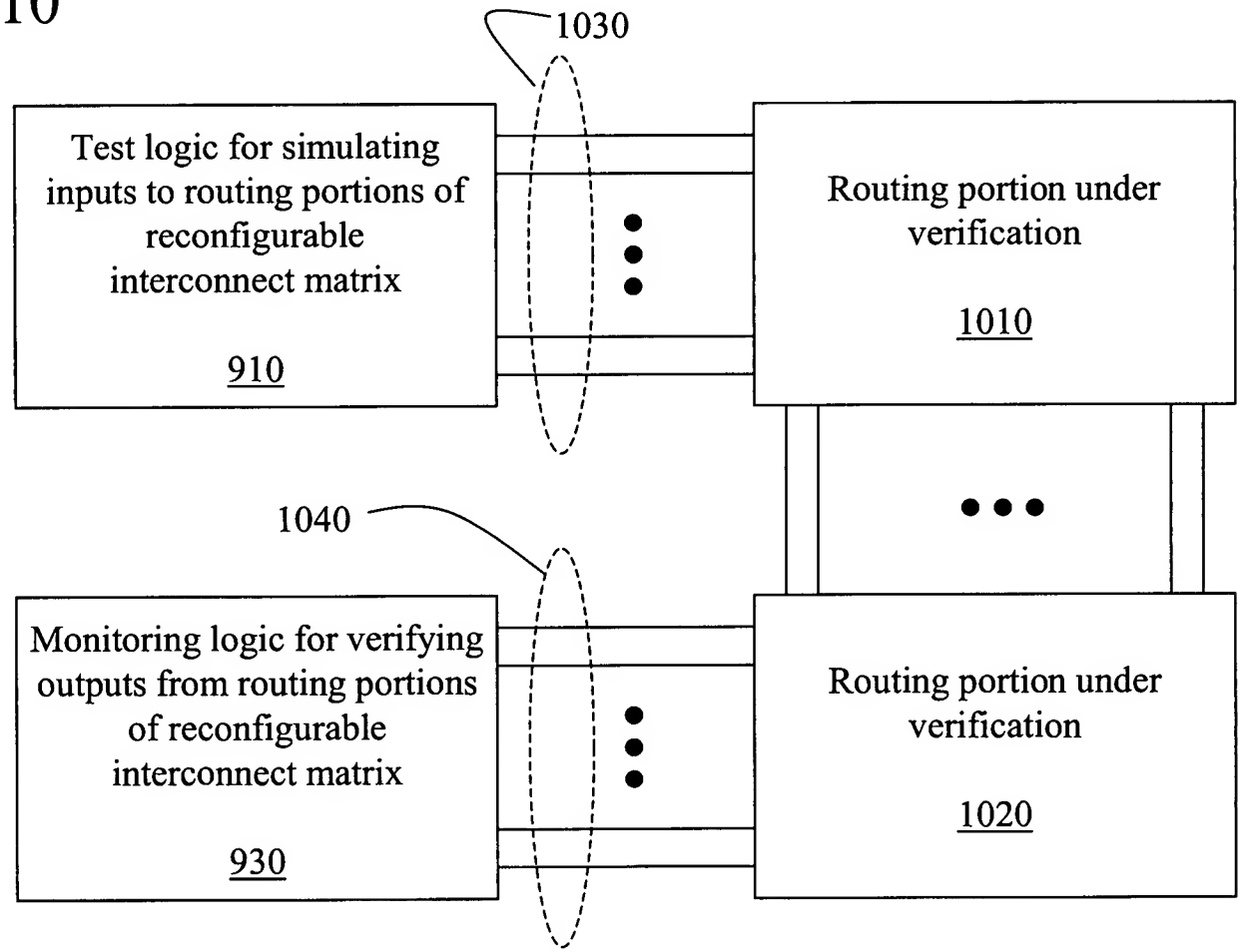

1030
Test logic for simulating inputs to routing portions of reconfigurable interconnect matrix
910
Routing portion under verification
1010
1040
Monitoring logic for verifying outputs from routing portions of reconfigurable interconnect matrix
930
Routing portion under verification
1020

Figure 11A

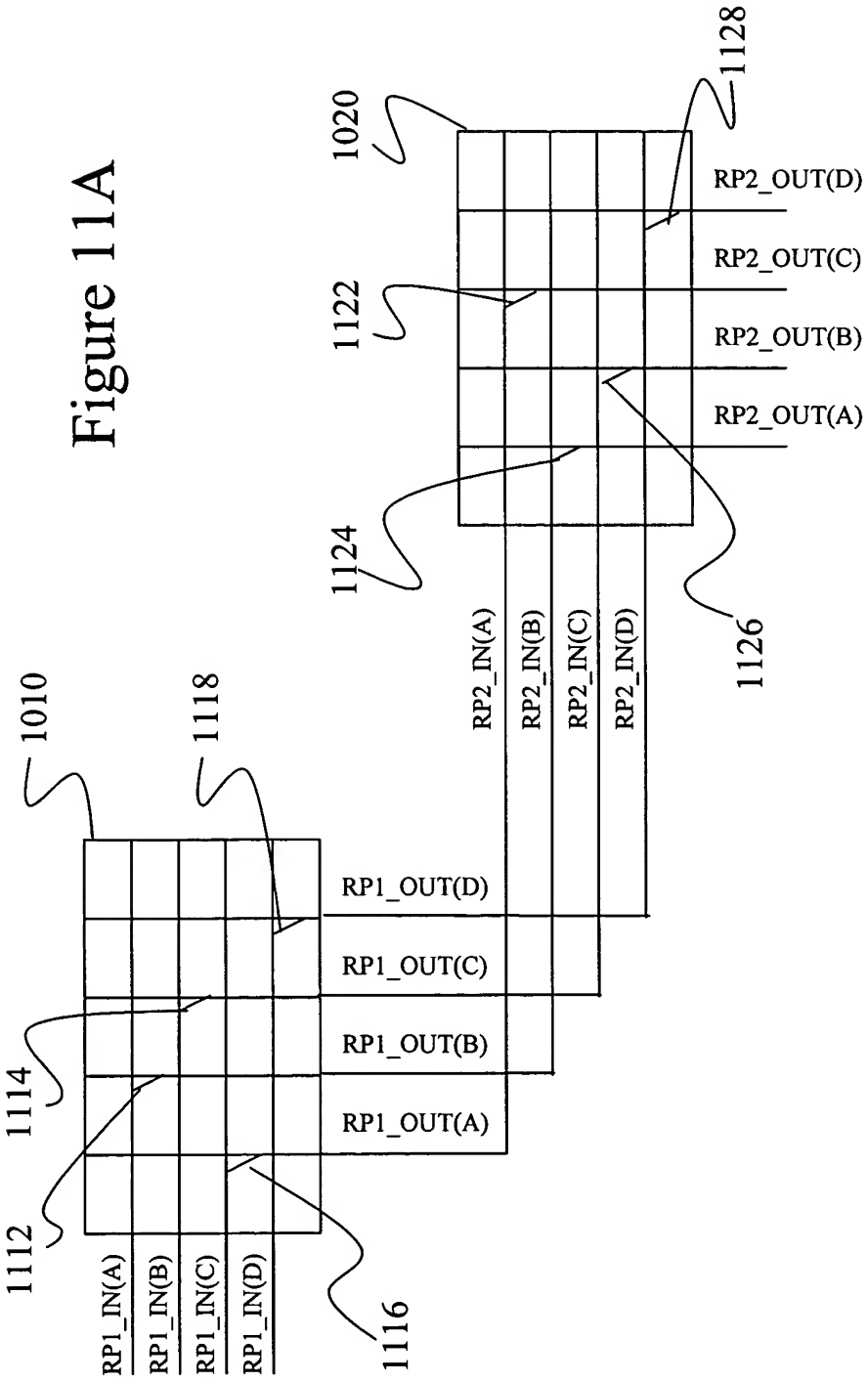

1010
1118
1020
1128
1122
1124
1126
1114
1112
1116
RP1_IN(A)
RP1_IN(B)
RP1_IN(C)
RP1_IN(D)
RP1_OUT(D)
RP1_OUT(C)
RP1_OUT(B)
RP1_OUT(A)
RP2_IN(A)
RP2_IN(B)
RP2_IN(C)
RP2_IN(D)
RP2_OUT(D)
RP2_OUT(C)
RP2_OUT(B)
RP2_OUT(A)

Figure 11B

	Input RP1	Output RP1
1112	A	B
1114	B	C
1116	C	A
1118	D	D

Figure 11C

	Input RP2	Output RP2
1122	A	C
1124	B	A
1126	C	B
1128	D	D

Figure 12

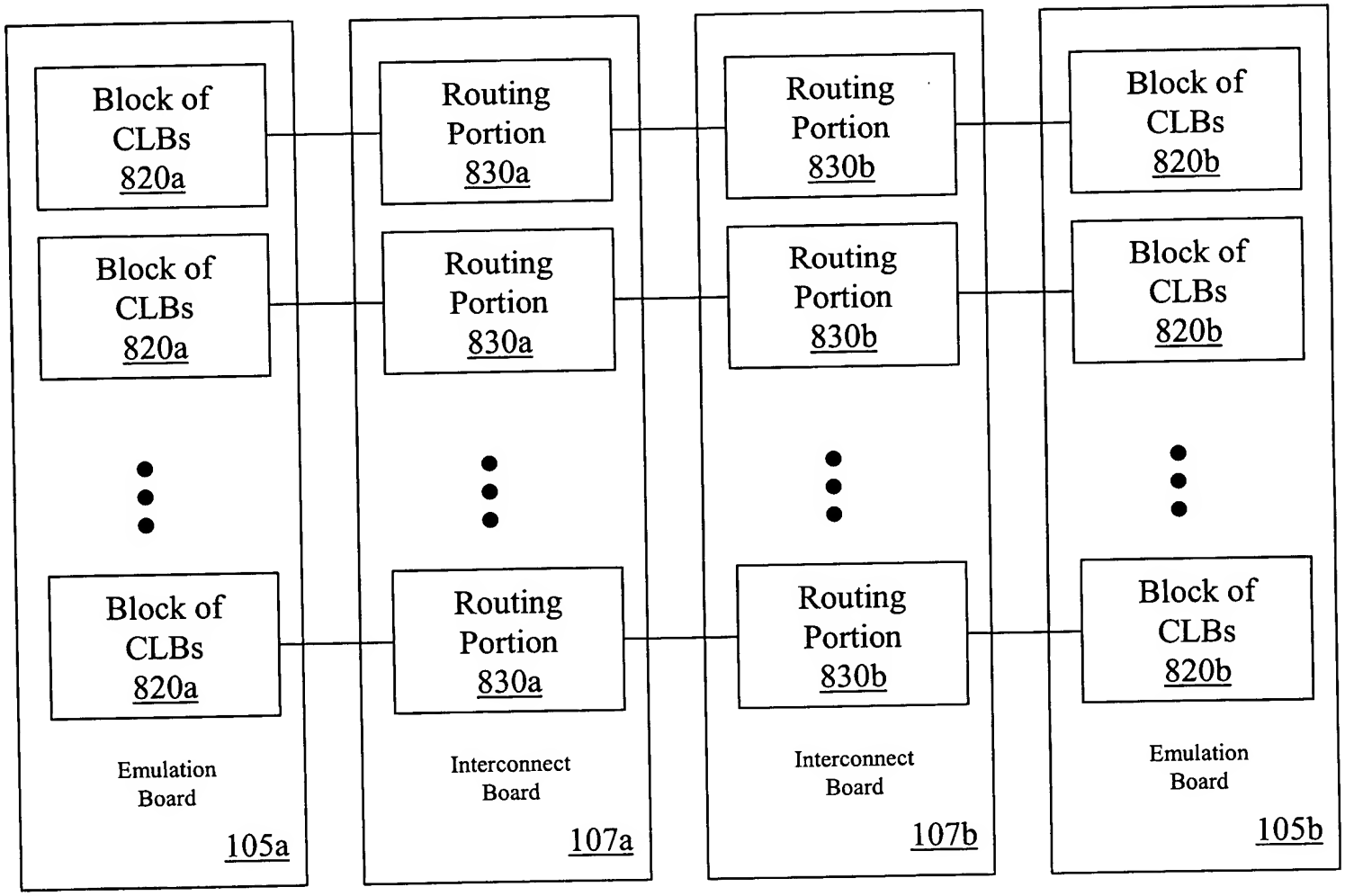

Block of CLBs 820a
Block of CLBs 820a
Block of CLBs 820a
Emulation Board 105a
Routing Portion 830a
Routing Portion 830a
Routing Portion 830a
Interconnect Board 107a
Routing Portion 830b
Routing Portion 830b
Routing Portion 830b
Interconnect Board 107b
Block of CLBs 820b
Block of CLBs 820b
Block of CLBs 820b
Emulation Board 105b

Figure 13A

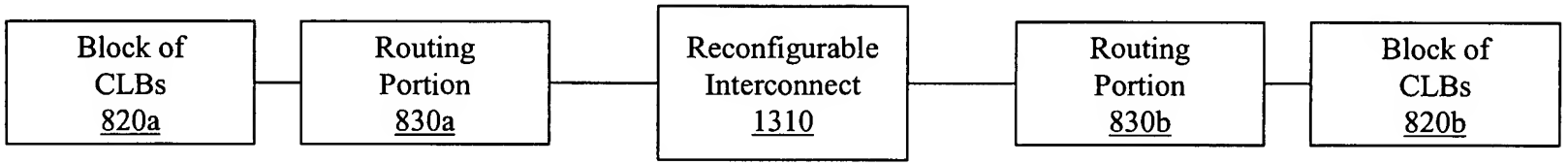


Figure 13B

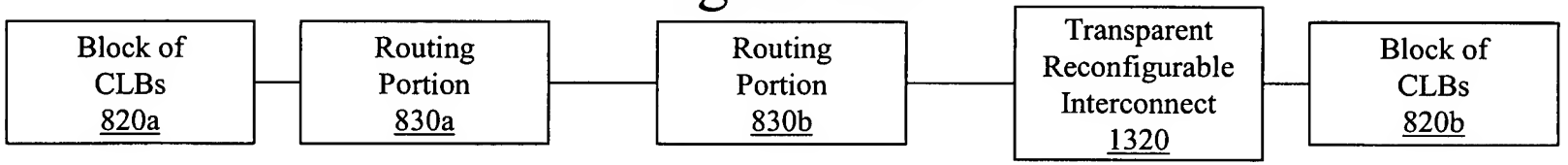


Figure 13C